Asmita Pal

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Education

PhD in Computer Engineering
University of Wisconsin - Madison *August'18 - Present*
Advisor : Prof. Joshua San Miguel

MS in Computer Engineering
Utah State University *August'16 - August '18*
Advisor : Prof. Koushik Chakraborty, Prof. Sanghamitra Roy

B.Tech. in Electronics and Instrumentation Engineering
West Bengal University of Technology, India *July'10 - June'14*

Publications

- **Asmita Pal**, Keerthana Desai, Rahul Chatterjee, Joshua San Miguel: **Camouflage: Utility-Aware Obfuscation for Accurate Simulation of Sensitive Program Traces**, published in ACM Trans. Archit. Code Optim. 21, 2, Article 36 (June 2024), 23 pages.
- Mitali Soni, **Asmita Pal**, Joshua San Miguel: **As-Is Approximate Computing**, published in ACM Trans. Archit. Code Optim. 20, 1, Article 3 (March 2023), 26 pages.
- **Asmita Pal**, Karthik Swaminathan, Subhankar Pal, Joshua San Miguel: **Characterizing Memory side channels in FHE applications** presented in DISCC Workshop *(held in conjunction with MICRO'22)*
- Pramesh Pandey, **Asmita Pal**, Koushik Chakraborty, Sanghamitra Roy: **Reliability and Uniformity Enhancement in 8T-SRAM based PUFs operating at NTC**, published in IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED) 2018.
- **Asmita Pal**, Aatreyi Bal, Koushik Chakraborty, Sanghamitra Roy: **Split Latency Allocator: Process Variation-Aware Register Access Latency Boost in a Near-Threshold Graphics Processing Unit**, published in J. Low Power Electronics 13(3): 419-427 (2017).

Awards

- Winner of N+1 Google AI Sustainability Competition at UW-Madison.
- Sarah and David Epstein Teaching Fellowship [Awarded by Department of Electrical and Computer Engineering, **UW-Madison**]
- Student Research Grant [Awarded by Office of Diversity, Inclusion and Funding at **UW-Madison**]
- Anita Borg Grace Hopper Celebration 2019 Scholarship
- Wisconsin Distinguished Fellow - Schneider [Awarded by Department of Electrical and Computer Engineering, **UW-Madison**]
- Rajendra Prasad and Yasoda Mani Grandhi Fellow [Awarded by Department of Electrical and Computer Engineering, **Utah State Uniersity**]

Experience

University of Wisconsin - Madison — Wisconsin, United States
Graduate Research Assistant August '18 – Present

- Identify possible timing side-channel leakage in Network-on-Chips or interposer-based systems.
- Architectural characterization of memory side-channels in applications encrypted using Fully Homomorphic Encryption.
- Privacy preserving synthetic trace generation by leveraging program semantics.
- Identifying patterns in memory accesses and impact of learning techniques on the same.
- Investigating workloads amenable to approximate computing for approximation-aware architectures.

AMD Research — Boston, United States
Research Intern — June '22 – Sept '22
- Worked on LLC management guided by modelling data reuse behavior.

AMD Research — Boston, United States
Research Intern — September '20 – December '20
- Worked on profiling memory bound, CPU-based AI applications to identify potential for acceleration.

Utah State University — Utah, United States
Graduate Research/Teaching Assistant — August '16 – July '18
- Investigated power-performance trade-off characteristics for present day processors, including both GPU and CPU.
- Cross-layer analysis of the effects of process variation on a GPU register file, represented by 10T-SRAM cell, operating at Near Threshold Voltages.
- Studied efficacy of different thread criticality metrics in multi-core systems.
- Analyzing role of Deep Neural Machine learning in image recognition and speaker identification problems.
- **Teaching** - High Performance Computer Architecture(ECE-5750)

Infosys Technologies Limited — Pune, India
System Engineer — July '14 – August'16
- Functioned as a team lead, and dealt with client deadlines and service delivery.
- Developed a project specific Automation Tool to enhance team productivity by amortizing the manual verification of device configurations.

Recent Projects

Side-channel attacks for Mesh-based Network-on-Chips(NOC) — Dec '23 – Present
Supervisor : Prof. Joshua San Miguel
- Identifying contention in mesh interconnect.
- Applying temporal partitioning mechanisms to overcome observed contention.

Characterizing Memory Side Channels of FHE Applications — Dec '21 – Dec'23
Supervisor : Prof. Joshua San Miguel
- Analyzing side channels in applications encrypted using FHE (Fully Homomorphic Encryption).
- Studying memory access patterns to understand vulnerability of operations in FHE domain.

Privacy-preserving Traces by leveraging Program Semantics — Jan '20 – Oct '23
Supervisor : Prof. Joshua San Miguel
- Characterized inherent architectural properties of program structures that influence program behavior, captured in traces.
- Proposed a trace-based obfuscation mechanism focused on program-semantic specific obfuscation techniques, with a security-conservative mindset.
- Developed a generalized threat model based on input indistinguishability to ensure input secrecy.

Analyzing patterns in memory accesses — Sep '18 – Dec '19
Supervisor : Prof. Joshua San Miguel
- Understanding impact of program structure on memory accesses and leveraging that to generate synthetic traces.
- Applying sequence prediction problem of natural language processing framework to memory access sequences.

Architectural Support for Anytime Approximate Computing — Jan '19 – Nov '19
Supervisor : Prof. Joshua San Miguel
- Design of speculation based architecture for anytime approximate computing.
- Characterizing approximate applications for an interruptive system to accommodate different levels of accuracy with runtime.

Digit Recognition on FPGA using Multilayer Perceptron Sep '19 – Dec '19

Supervisor : Prof. Parmesh Ramanathan

- Design of processor, memory and accelerator modules to enable storage of a pre-trained model and offload computations to accelerator.
- Facilitating timely image capture and display of recognized image on the 7-segment display.

Precise encoding in Stochastic Computing for Neural Networks Sep '18 – Dec '18

Supervisor : Prof. Younghyun Kim

- Proposed of a new encoding scheme for Stochastic Numbers and implemented this new encoding format in MAC module of a small scale Neural Network.
- Analyzed the energy-accuracy trade-off for LeNet300-100 and observed upto 5X energy degradation.

Design of a Process-Variation Aware Low Power GPU Jan '17 – July '17

Supervisor : Prof. Koushik Chakraborty, Prof. Sanghamitra Roy

- Explored the factors affecting the operation of a GPU at Near Threshold Voltages, especially the role of process variation on register files.
- Analyzed the performance variation in GPGPU applications from AMD APP SDK suite, with varying register latency.
- Proposed a low overhead technique to overcome the effects of process variation on register latency. Exhibited ∼36% reduction in GPU energy consumption with marginal area and power overheads.

Speaker Diarization using Deep Neural Networks Sep '17 – Dec '17

Supervisor : Prof. Todd Moon

- Extracted features from a conversation and use Deep Neural Networks to separate this audo signal into its homogeneous components according to speaker identity.
- Presented a comparative performance evaluation in the speaker diarization framework, using deep neural networks and convolutional neural networks (max prediction accuracy ∼89%).

Critical Thread Predictor Jan '17 – April '17

Supervisor : Prof. Koushik Chakraborty

- Illustrated the statistical coherence of thread criticality metrics based on cache-misses and synchronization bottlenecks and discussed the scope of performance optimization.
- The simulations were executed on a multi-core CPU, modelled on Intel Nehalem architecture, running applications from Splash2 Benchmark suite.

GPU Power and Area Analysis Jan '17 – April '17

Supervisor : Prof. Sanghamitra Roy

- Synthesis, place and route for basic pipe stages of a GPU, to study of change in power and area and timing violation, with frequency and technology node variation.

Design of a Global Router Aug '16 – Dec'16

Supervisor : Prof. Sanghamitra Roy

- Developed a VLSI floorplan based on simulated annealing algoritm.
- Implemented a global routing engine using A* search algorithm

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Professional Service

Invited Talks

- University of Central Florida - Computer Architecture Coordination Seminar Series, November 2023

Artifact Evaluation Committee

- IEEE/ACM International Symposium on Microarchitecture 2023 (MICRO 2023, 2022)
- Architectural Support for Programming Languages and Operating Systems (ASPLOS 2022)
- Conference on Machine Learning and Systems (MLSys 2020)
- Architectural Support for Programming Languages and Operating Systems (ASPLOS 2020)

Teaching

- TA for ECE352(Digital System Fundamentals) and ECE757(Advanced Computer Architecture)

Research Interests

- Computer Architecture
- Synthetic Trace Generation
- Data Privacy
- Caches and Memory Access Patterns

Relevant Coursework

University of Wisconsin - Madison — Wisconsin, United States

Advanced Computer Architecture, Introduction to OS, Embedded Computing Systems, Security and Privacy

Utah State University — Utah, United States

High Performance Computer Architecture, Parallel Computer Architecture, VLSI Design Automation, Neural Networks, Advanced Algorithms